REMARKS

In the Office Action mailed June 23, 2005, the Examiner objected to claims 15-23; rejected claim 10 under 35 U.S.C. § 112, second paragraph; rejected claims 1-7 and 14 under 35 U.S.C. § 102(b); and rejected claims 8-13 under 35 U.S.C. § 103(a). Claims 1-23 remain pending and under consideration.

Response to § 102 Rejections

The Examiner rejected claims 1-7 and 14 under 35 U.S.C. § 102(b) as anticipated by U.S. Patent No. 4,439,864 ("Qureshi"). These rejections are respectfully traversed.

Claims 1 and 6 recite "delaying . . . [an] analog signal corresponding to a latency caused by the generation of . . . [a] control signal." Qureshi does not teach this feature.

The Examiner appears to assert on page 3 of the Office Action that either the text in column 6 at lines 15-42 discloses this feature or crystal oscillator 96 corresponds to this feature. The text in column 6 describes filters implemented by central microprocessor (MPU) 30 and illustrated in Figure 7 as parts 232, 234, and 236. This text cannot teach this feature of claim 1. First, none of these filters receive an analog signal. Instead they receive a digital signal from A/D converter 64 (see column 6, lines 15-16). Second, although these filters have delay units such as delays 238, 254, and 264, these delays clearly do not delay "corresponding to a latency caused by the generation of . . . [a] control signal to generate a delayed analog signal." Qureshi does not describe in detail the characteristics of these delays. Regarding crystal oscillator 96, this component merely provides the clocking signal used by the circuit. Use of an oscillator does not correspond to the feature of claim 1 recited above. As no other portions of Qureshi teach anything comparable to this feature of claim 1, claim 1 is patentable over Qureshi.

Claim 7 recites "delaying . . . [an] analog signal corresponding to a latency caused by the ADC and . . . [a] digital arithmetic circuit to generate a delayed analog signal." Qureshi does not teach this feature.

On page 4, line 6 of the Office Action, the Examiner asserts that Qureshi discloses this feature in column 6, lines 15-20 and column 4, lines 8-20. As previously explained, the text in column 6, lines 15-20 does not disclose anything comparable to this feature. Regarding the text in column 4, this text primarily relates to gain control factors. Although this text teaches "buffering each incoming rk^m input from A/D converter 64," nothing taught in this text is comparable to this feature as discussed above with respect to claim 1. As no other portions of Qureshi teach anything comparable to this feature of claim 7, claim 7 is patentable over Qureshi.

If there are any additional fees associated with filing of this Amendment, please charge the same to our Deposit Account No. 19-3935.

Respectfully submitted,

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